REMARKS

Claims 1-23 are pending in the current Application. No Amendments to the claims are being made herein.

Applicants respectfully submit that claims 1-23 are patentable under 35 U.S.C. 103(a) over Macon et al. (US 5410653) in view of Hussain et al. (US 6901500). With respect to claim 1, Applicants submit that neither Macon, Hussain, nor their combination, teach or suggest each and every element of claim 1. Applicants have amended claim 1 to clarify that "when a hit occurs in the prefetch buffer *and* a total number of prefetches that have occurred since a previous miss in the prefetch buffer has reached the first prefetch limit, a prefetch does not occur in response to the hit." This amendment was made to further clarify how the prefetch limit operates to control how many prefetches occur between misses in the prefetch buffer and not for prior art reasons. Applicants submit that at least this is not taught or suggested by the cited references. The Examiner cites FIG. 6 of Macon and column 5, lines 45-65, and states that Lmax teaches the first prefetch limit. However, Applicants respectfully disagree. Firstly, Lmax is simply a max value for L, where L indicates how many contiguous data blocks are to be fetched during a subsequent prefetch. However, even if L reaches Lmax, and is held at Lmax, a prefetch of Lmax units (in block G) can *continue to occur upon* ***hits*** *in the MRRS*. L thus does not limit a number of prefetches which occurs between misses because any number of prefetches can occur between misses in Macon. That is, there is never a point in Macon where, based on the value of L or Lmax being reached, prefetches *no longer occur upon a hit* because L does not provide a prefetch limit as claimed. For example, the prefetch of L units (even if L=Lmax) in block G in FIG. 6 can occur any number of times between misses because *so long as hits in the MRRS continue*.

The Examiner, in point B of his response to arguments in the current Office Action, states that "there is not any limitation in the claim that requires the prefetching to stop when reaching a prefetching value." However, although Applicants disagree, Applicants have amended claim 1 as stated above to explicitly include "when a hit occurs in the prefetch buffer and a total number of prefetches that have occurred since a previous miss in the prefetch buffer has reached the first prefetch limit, a prefetch does not occur in response to the hit." That is, the prefetching of claim 1 can stop when the total number of prefetches since a previous miss reaches the prefetch limit,

which is clearly not taught or suggested by Macon, as discussed above in the previous paragraph. For example, referring again to Macon, so long as hits in the MRRS continue, a prefetch is performed at block G. Also, Hussain also does not teach or suggest the prefetch limit of claim 1, and therefore, Applicants submit that for at least these reasons, claim 1 is allowable over the cited references.

Claims 2-9 are not being independently addressed because they depend directly or indirectly from allowable claim 1 and are therefore allowable for at least those reasons provided above with respect to claim 1.

With respect to claim 10, Applicant has also amended claim 10 to clarify the prefetch limit in a manner similar to the amendments to claim 1. That is, claim 10 clarifies that "when a hit occurs in the prefetch buffer and a total number of prefetches that have occurred since a previous miss in the prefetch buffer has reached the first prefetch limit, a prefetch does not occur in response to the hit." Applicants submit that at least this is not taught or suggested by the cited references. The reasons provided above with respect to claim 1 also apply here to claim 10. Therefore, for at least these reasons, Applicants submit that claim 10 is allowable over the cited references.

Claims 11-14 are not being independently addressed because they depend directly or indirectly from allowable claim 10 and are therefore allowable for at least those reasons which apply to claim 10.

Comments Regarding Granted Petition

Applicants' Petition submitted January 7, 2005 was granted on September 16, 2005, granting a filing date of July 31, 2003. However, Applicants note that the filing date in the Office Action mailed July 28, 2006 is still incorrectly provided as September 9, 2004. Applicants request that the filing date be corrected accordingly.

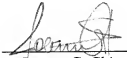
Conclusion

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants.

Applicants respectfully solicit allowance of the pending claims. Should there be any issues or questions regarding this communication or the current Application, please feel free to contact me.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

By: 

Joanna G. Chiu
Attorney of Record
Reg. No.: 43,629
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125